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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/660,254	GROEN ET AL.	
	Examiner	Art Unit	
	SOPHIA VLAHOS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-23* is/are pending in the application.

4a) Of the above claim(s) *2 and 24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 5/21/2007 addressing the rejection of claim 6 under 35 U.S.C 102(b) as being anticipated by Ducaroir et.al., (U.S. 2001/0043648) have been fully considered but they are not persuasive.

Applicant argues (page 7, second paragraph of section A. Claim 6) : "More specifically, Ducaroir teaches that Serializer 18 either uses either a reference clock signal to serialize the parallel data during non-test condition, or uses a recovered clock signal to serialize the parallel data during test condition (See Ducaroir, paragraph 0021))...Namely, Ducaroir does not teach or suggest using a recovered clock signal and a reference clock signal concurrently to perform processing functions as positively claimed by the Applicants."

Examiner disagrees with Applicant's assessment that the Ducaroir reference. does "not teach or suggest using a recovered clock signal and a reference clock signal concurrently to perform processing functions as positively claimed by the Applicants." The cited passage paragraph [0021] on which the Applicant relies to rebut the rejection describes the test-mode operation of the transceiver. However, the rejection of claim 6, relies on paragraph [0020] where the normal mode of operation of the transceiver is described. Specifically, paragraph [0020] (lines 9-end of praragraph). Therefore, as described in paragraph [0020] in a normal operating mode, lines 16-18, 21-23, the receiver 14, receives a serial data stream and recovers a 'recovered clock' signal that is used to synchronize the operation of the receiver. With respect to the claimed

reference clock signal, see paragraph [0021] lines 9-16, where the operations of the transmitter (in normal mode) are synchronized by a supplied 'reference clock'. Since Ducaroir does not provide any details regarding a "second circuitry" used to generate the "refrence" clock signal (just an input port where the reference clock is provided), the rejection under 35 U.S.C 102(b) is withdrawn and new grounds of rejection is made based on 35 U.S.C 103(a).

2. Applicant's arguments filed 5/21/2007 addressing the rejection of claims 8-9, 22-23 under 35 U.S.C 102(e) as being anticipated by Ziegler et. al., (U.S. 2003/0112798) have been fully considered but they are not persuasive.

With respect to the rejection of claim 8, Applicant argues: "Namely, Ziegler does not teach or suggest using a plurality of recovered clock signals from a plurality of serial data and a reference signal as positively claimed by the Applicants." As well as " Since Ziegler does not teach an approach where a plurality of recovered clocks and a reference clock are provided to a circuit portion where one of the clocks is used for processing one of the serial data, Ziegler does not teach each and every element of Applicants' independent claim 8. Accordingly, Ziegler does not anticipate Applicants' invention as recited in claim 8."

Examiner disagrees with the aforementioned Applicant arguments. Specifically, Ziegler teaches recovering a plurality of recovered clocks (clocks 310, and 330 as shown in Fig. 3 and paragraph [0025] and see paragraph [0024] where Fig. 3 discloses the parallel data reassembly using at least the reference clock out of block 322).

Therefore the rejection of claims 8 and 22 (similar arguments were presented by the Applicant with respect to the rejection of claim 22) is maintained. See that Ziegler discloses (with respect to claim 22) concurrently performing processing functions in the processing blo0ck using the first and second clocks and the reference clock (see Fig. 3, use of recovered clocks 310 and 330 and reference clock out of block 322).

3. Applicants Applicant's arguments (pages 10-15 addressing the rejection of claims 1, 3-5, 7, 10-21), filed 5/21/2007,have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Desai (U.S. 6,288,656) and Mann et. al., (U.S. 5,251,210).

The indicated allowability of Claim 23 is withdrawn.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 4, 6-7, 22, 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Desai (U.S. 6,288,656).

With respect to claim 1, Desai discloses: first clock data recovery circuitry for receiving first serial data and recovering a first recovered clock from the first serial data (see Fig. 7, Channel 1, serial data RXD1 and block 706 "Clock Recovery", outputting a first recovered clock from the first serial data RXD1, column 1, lines 7-8 where the invention relates to a transceiver, column 5, lines 45-59); a second clock data recovery circuitry for receiving second serial data and recovering a second recovered clock from the second serial data (Fig. 7, Channel 2, serial data RXD2 and block 706 "Clock Recovery", outputting a first recovered clock from the first serial data RXD2, column 5, lines 45-59); wherein the transceiver provides the first recovered clock, the second recovered clock, a reference clock, the first serial data and the second serial data to a circuit portion of the transceiver (Fig. 7 circuit portion to the right of FF block 704, the recovered clocks of channels 1, 2, and one of the channel word clock(s) corresponding to the reference clock that is used to deserialize the data into parallel data words , (see column 4, lines 32-34), RXD1, RXD2 serial streams), wherein the circuit portion uses one of the first recovered clock, the second recovered clock and the reference clock (see Fig. 7, where the respective recovered clocks retime the RXD1 and RXD2 streams, and Channel Word Clock, is used in DMUX to convert the retimed serial data into parallel words) for subsequent processing of one of the first serial data and the second

serial data (see Fig. 2 where for channel 1, the first recovered clock and the channel word clock (the reference clock) are used to process the RXD1 data, and a similar processing takes place for channel 2).

With respect to claim 4, Desai discloses: wherein the first serial data is an receive serial bit stream (see column 5, lines 45-49).

With respect to claim 6, Desai discloses: first circuitry for receiving first serial data and recovering a first recovered clock based on the first serial data (Fig. 7, see first serial data RXD1 of Channel 1, and recovered clock out of block 706), wherein the first circuitry provides the first recovered clock to a first clock based functionality (the first recovered clock supplied to CLKGEN 710 (the first clock based functionality) in the Channel 1, processing side); and second circuitry for generating and providing a reference clock to a second clock based functionality (see the channel word clock (the reference clock) that clocks DMUX 708, (the second clock based functionality); and wherein the first and second clock based functionalities concurrently perform processing functions (see that the CLKGEN and the clocking of the DMUX, operate concurrently) using the first recovered clock and the reference clock, respectively.

With respect to claim 7, Desai discloses: further comprising third circuitry for receiving second serial data and recovering a second recovered clock based on the second serial data (see Channel 2 side of Fig. 7, receiving second serial data stream RXD2, and block 706 clock recovery outputting a second recovered clock), wherein the

circuitry provides the second recovered clock to a third clock based functionality (CLKGEN 710 in Channel 2 side), and wherein the first, second and third clock based functionalities concurrently perform processing functions using the first recovered clock, the reference clock and the second recovered clock, respectively (see column 5, lines 9-11, see the parallel (concurrent) processing).

With respect to claim 22, Desai discloses: receiving a first data stream and recovering a first clock based on the first data stream (see Fig. 7, serial data RXD1 of Channel 1, and clock recovery block 706); providing the first clock to a first circuit portion (Fig. 7 recovered clock is supplied to FF 704) ; receiving a second data stream and recovering a second clock based on the second data stream (see RXD2 serial data for Channel 2, and recovered clock out of clock recovery block 706 of channel 2); providing the second clock to a second circuit portion (see Fig. 7, FF 704 of Channel 2); providing a reference clock to a third circuit portion (clock out of CLKGEN 710 (Channel 1 and/or Channel 2 that provides a reference clock (Channel Word Clock) controls Dmux); and concurrently performing processing functions in the processing block using the first and second clocks and the reference clock (the recovered clocks are used to trigger the CLKGEN that generate the Channel word clock).

With respect to claim 23 Desai discloses: receiving a plurality of input data streams (see Fig. 7, RXD1, RXD2, column 5, lines 40-45);recovering a corresponding

plurality of clocks based on the plurality of input data streams (see Fig. 7, clock recovery blocks for each serial data stream channel); determining at least one output port for providing outgoing data streams (see Fig. 7, the compare blocks that control the muxes that output the recived data, column 6, lines 36-41, selection of appropriate bits for output); and providing each input data stream of the plurality of input data streams to the at least one output port based upon each corresponding recovered clock of the corresponding plurality of recovered clocks (see Fig. 7 where the recovered clocks are used to retime the serial data streams using the FF 704, column 5, lines 53-54); wherein the at least one output port comprises a number of output ports that corresponds to a number of input data streams of the plurality of input data streams (see Fig. 7 two outputs (output ports) one for each channel), and wherein the method further comprises determining, for each input data stream of the plurality of input data streams, an output port and providing each input data stream of the plurality of input data streams to the determined output ports based upon each corresponding recovered clock of the corresponding plurality of recovered clocks (see Fig. 7, outputting the received data 8 bits using the mux, compare and state machine, to select the 8 bits from the 12 bit supplied to muxes).

6. Claims 1, 4-7, 10-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Mann et. al., (U.S. 5,251,210).

With respect to claim 1, Mann et. al., disclose: first clock data recovery circuitry for receiving first serial data and recovering a first recovered clock from the first serial

data (Fig. 7, see Channel 1,blocks 260, 250, see column 14, lines 28-39, for serial data streams see column 6, lines 39-43); a second clock data recovery circuitry for receiving second serial data and recovering a second recovered clock from the second serial data (Fig. 7, see Channel 2 blocks 260 and 250); wherein the transceiver provides the first recovered clock, the second recovered clock, a reference clock, the first serial data and the second serial data to a circuit portion of the transceiver (see column 1, lines 9-11, transmitting/receiving communication system (transceiver) and Fig. 7 (the receiver side), see circuit portion including block 240, fifos 210, (and blocks to the right of the fifos, see column 13, lines 54-67, column 14,lines 1-15, and the reference clock is clock RxCLK out of block 240, used to recombine the serial streams, see column 15, lines 34-39); and wherein the circuit portion uses one of the first recovered clock, the second recovered clock and the reference clock for subsequent processing of one of the first serial data and the second serial data (see Fig. 7, see that the recovered clocks are used in corresponding FIFOs to retime the serial data streams (column 14, lines 40-52), and the reference clock (RxCLK) is used in combiner (column 15, lines 32-39)).

With respect to claim 4, Mann et. al., disclose: wherein the first serial data is an receive serial bit stream (see column 3, lines 63-65 description of Fig. 7, and column 6, lines 39-43 where the first serial data of Fig. 7 (Channel 1 RxDATA) is a receive serial bit stream).

With respect to claim 5, Mann et. al., disclose: wherein the circuit portion comprises a portion of a programmable logic fabric (Fig. 7, block 240 "Reassembly Control Logic", see column 16, lines 39-44, the operation of block 240 implemented by a microprocessor or custom logic (any one of these corresponds to the claimed programmable logic fabric)).

With respect to claim 6, Mann et. al., disclose: first circuitry for receiving first serial data and recovering a first recovered clock based on the first serial data (Fig. 7, Channel 1, RxDATA blocks 260 and 250, column 14, lines 28-33, and column 6, lines39-43 see serial data streams)wherein the first circuitry provides the first recovered clock to a first clock based functionality (Fig. 7, recovered clock CLK of Channel 1 is supplied to FIFO 210 of Channel 1); and second circuitry for generating and providing a reference clock to a second clock based functionality (see Fig. 7, CLK1 out of block 240, column 15, lines 58-65, where the one of the generated CLK1-CLKN corresponds to the claimed reference clock, supplied to FIFO 210); and wherein the first and second clock based functionalities concurrently perform processing functions using the first recovered clock and the reference clock, respectively (column 16, lines 9-15, the FIFO clocking using the first recovered, and suppression of clock pulses using the reference clock CLK1) .

With respect to claim 7, Mann et. al., disclose: further comprising third circuitry for receiving second serial data and recovering a second recovered clock based on the second serial data (Fig.7, channel 2 components 260, and 250 that have the same

function as the corresponding components of Channel 1), wherein the circuitry provides the second recovered clock to a third clock based functionality (Fig. 7, FIFO 210 of Channel 2), and wherein the first, second and third clock based functionalities concurrently perform processing functions using the first recovered clock, the reference clock and the second recovered clock, respectively (Fig. 7, timing respective FIFOs using the first , second recovered clocks and the reference clocks).

With respect to claim 10, Mann et.al., disclose: clock recovery circuitry coupled to receive a high data rate input data stream (Fig. 7, blocks 250 of the received data channels, see column 5, lines 52-53 the 1.536 megabit rate), wherein the clock recovery circuitry recovers a recovered clock based on the high data rate input data stream (Fig. 7, function of CLK recovery blocks 250, where the recovered clock is the clock that is received by receiver and is recovered using block 250); and a programmable logic fabric portion wherein the programmable logic fabric portion performs subsequent processing based on one of the recovered clock and a reference clock (Fig. 7, block 240, the recovered clock(s) are supplied to block 240, that controls the FIFOS -that are used for subsequent processing, see column 15, lines 58-65, and column 16, lines 39-44, the reassembly process implemented using a microprocessor or custom logic (any one of these corresponds to the claimed programmable logic fabric).

With respect to claim 11, Mann et. al., disclose: wherein the high data rate input data stream is received according to a first protocol and is converted to a second

protocol by the programmable logic fabric portion based on the recovered clock (see Fig. 7, where the high data rate input data stream is a serial data stream (first protocol) and is retimed using respective FIFO 210 (second protocol) using CLK1 output by programmable logic fabric (240) and (CLK1 is generated based on the recovered clock of Channel 1 , see column 15, lines 58-65, and column 16, lines 8-15).

With respect to claim 12, Mann et. al., disclose: further comprising transmit circuitry coupled to receive the converted high rate input data stream in the second protocol (Fig. 7, combiner (reassembling the data stream(s)) 230, that sends the RxDATA to the user interface), wherein the programmable logic fabric portion provides the converted high data rate input data stream in the second protocol based on the recovered clock (see above rejection of claim 11).

With respect to claim 13, Mann et. al., disclose: further comprising a second clock recovery circuit for recovering a second recovered clock based on an I/O serial data stream (Fig. 7, Channel 2 processing of serial RxData, similar to the processing of Cahnnel 1, serial data as explained in the rejection of claim 10 above).

With respect to claim 14, Mann et. al., disclose: receiving a high data rate input data stream; recovering a recovered clock based on the high data rate input data stream (Fig. 7, Channel 1, blocks 260, 250 receiving Channel 1 data see column 5, lines 52-53 the 1.536 megabit rate); providing the recovered clock to a programmable

logic fabric portion (block 240, the programmable logic fabric, receives the recovered clock from Channel 1. block 250, column 15, lines 58-65, column 16, lines 39-44); and performing subsequent processing in the programmable logic fabric portion based on the recovered clock (see column 15, lines 58-65, where the recovered CLK is used by block 240 to generate CLK1).

With respect to claim 15, Mann et. al., disclose: wherein the high data rate stream is received according to a first protocol (see column 6, lines 410-43, the received RxData of Channel 1 has serial format (first protocol), see column 6, lines 40-43).

With respect to claim 16, Mann et. al., disclose: wherein the high data rate input data stream is converted to a second protocol based on the recovered clock (see Fig. 7, combiner 230, reassembles (combines) the high data rate stream (of Channel 1 for example) with other data streams, i.e. conversion to a second protocol (reassembled data)).

With respect to claim 17, Mann et. al., disclose: wherein the recovered clock is a first recovered clock (see Fig. 7, Channel 1, processing blocks, CLK is a first recovered clock (of Channel 1)),further comprising recovering a second recovered clock based on a transmitter clock,(Fig. 7, other Channel clock recovery blocks 250, that recover respective CLK, (see column 19, lines 3-7 the 1.544MHz, second recovered clock and

see Fig.5, transmitter side where a transmitter clock out of 110 is used to clock the transmitted data in the respective Channels).

With respect to claim 18, Mann et. al., disclose: further comprising transmitting the converted data rate input data stream in the second protocol based on the second recovered clock (column 15, lines 58-67, the second recovered clock is used to generate CLK2 that is used in the FIFO of Channel 2 and the Alignment & Alignment monitor pattern detector 220, whose output is used in the conversion to the second protocol).

With respect to claim 19, Mann et. al., disclose: receiving a first serial bit stream and recovering a first recovered clock from the first serial bit stream (Fig. 7, Channel 1, RxData, CLK out of block 250 of Channel 1); receiving a second serial bit stream and recovering a second recovered clock from the second serial bit stream (Fig. 7, Channel 2, RxData, CLK out of block 250 of Channel 2); providing the first and second recovered clocks and a reference clock to a circuit portion (Fig. 7, see circuit portion including elements 210, 220, 230, (of all Channels) as well as block 240, that receive the first and second recovered clocks, and RxCLK (the reference clock used to reassemble the RxData); and within the circuit portion, choosing among the first and second recovered clocks and the reference clock for subsequent processing (Fig. 7, where the recovered clocks are supplied to 240, and are used to generate CLK1-CL2 (i.e. used for subsequent processing), see column 15, lines 58-65).

With respect to claims 20-21, Mann et.al., disclose: wherein the first serial bit stream is an receive serial bit stream (see column 6, lines 40-43); wherein the second serial bit stream is a transmit serial bit stream (again, column 6, lines 40-43, the RxxData serial channels).

With respect to claim 22, Mann et. al., disclose: receiving a first data stream and recovering a first clock based on the first data stream; providing the first clock to a first circuit portion; receiving a second data stream and recovering a second clock based on the second data stream; providing the second clock to a second circuit portion; providing a reference clock to a third circuit portion; and concurrently performing processing functions in the processing block using the first and second clocks and the reference clock

With respect to claim 23, Mann et. al., disclose: receiving a plurality of input data streams recovering a corresponding plurality of clocks based on the plurality of input data streams determining at least one output port for providing outgoing data streams; and providing each input data stream of the plurality of input data streams to the at least one output port based upon each corresponding recovered clock of the corresponding plurality of recovered clocks; wherein the at least one output port comprises a number of output ports that corresponds to a number of input data streams of the plurality of input data streams, and wherein the method further comprises determining, for each

input data stream of the plurality of input data streams, an output port and providing each input data stream of the plurality of input data streams to the determined output ports based upon each corresponding recovered clock of the corresponding plurality of recovered clocks

7. Claims 8, 9, 22, 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Ziegler et al. (U.S. Pub. No. 2003/0112798).

Claim 8, circuitry for receiving a plurality of input serial data streams (Ziegler discloses receiving a first serial bit stream ([0021], lines 1-2 and receiving a second serial bit stream [0021], lines 4-5); clock data recovery circuitry for recovering a corresponding plurality of recovered clocks based on the plurality of input serial data streams; circuitry for providing a reference clock.([0029], lines 1-3); and logic for selecting from the plurality of input serial data streams and for providing at least one outgoing serial data stream to an outgoing transmit block (Ziegler discloses recovering a first recovered clock from the first serial bit stream [0023], lines 39-41 and recovering a second recovered clock from the second Serial bit stream [0023], lines 42-44); wherein the logic provides each received input serial data stream of the plurality of input serial data streams to the outgoing transmit block based upon each corresponding recovered clock of the plurality of corresponding recovered clocks ([0021], lines 6-12).

Claim 9, Ziegler further discloses the outgoing transmit block is a transmitter port ([0021], lines 6-12).

Claim 22, Ziegler discloses receiving a first serialbit stream ([0021], lines 1-2) and recovering a first recovered clock from the first serial bit stream ([0023], lines 39-41); providing the first.clock to a first circuit portion ([0029], line 5-7, A-FIFO-1314 is controlled by first extracted clock); receiving a second serial bit stream ([0021], lines 4-5) and recovering a second recovered clock from the second serial bit stream ([0023], lines 42-44); providing the second clock to a second circuit portion ([0029], line 5-7, B-FIFO-1334 is controlled by second extracted clock); providing a reference clock to a third circuit portion ([0029], lines 1-3, A-FIFO-2318 and B-FIFO-2338 are controlled both by the same reference clock 322); and concurrently performing processing functions in the processing block using the first and second clocks and the reference clock ([0029], the read and write operations of both A and B FIFOs occur simultaneously).

Claim 23, Ziegler discloses receiving a plurality of input data streams (Ziegler discloses receiving a first serial bit stream ([0021], lines 1-2 and receiving a second serial bit stream [0021], lines 4-5); recovering a corresponding plurality of clocks based on the plurality of input data streams (Ziegler discloses recovering a first recovered clock from the first serial bit stream [0023], lines 39-41 and recovering a second recovered clock from the second serial bit stream ([0023], lines 42-44); determining at least one output port for providing outgoing data streams ([002], lines 6-12); and providing each input data stream of the plurality of input data streams to the at least one output port based upon each corresponding recovered clock of the corresponding plurality of recovered

clocks ([002], lines 1-12, each of the first and second serial data streams is clocked by the first and second recovered clocks, respectively).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ducaroir et. al., (U.S 2001/0043648).

Claim 6 Ducaroir discloses:

- first circuitry for receiving first serial data and recovering a first recovered clock based on the first serial data, wherein the first circuitry provides the first recovered clock to a first clock based functionality ([0020], lines 16-18, 21-23);
- providing a reference clock to a second clock based functionality ([0020], lines 14-16);
- the first and second clock based functionalities concurrently perform processing functions using the first recovered clock and the reference clock, respectively ([0020]).

Ducaroir does no expressly teach (show): second circuitry for generating and providing a reference clock signal. However, in the field of endeavor, circuitry for generating and

providing a reference clock signal, are known in the art, for example crystal oscillator circuitry (that generates and provides a reference clock signal). Therefore at the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Ducaroir, so that the reference clock signal is generated and provided by second circuitry (such as a crystal oscillator circuitry) and the rationale to perform such a modification is that crystal oscillator circuits generate a very precise frequency.

10. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Desai (U.S. 6,288,656) in view of Tang et. al., (U.S. 2002/0075981).

With respect to claim 3, Desai discloses: further comprising circuitry (see Fig. 7, block 706 on the Channel 2 processing side, receives RXD2 serial data stream) for receiving second serial data and produces a second recovered clock from the second serial data (see Fig. 2,ouput of block 706) in the transceiver provides the second serial data to the circuit portion and wherein the circuit portion (see circuit portion comprising components to the right of FF block 704) uses one of the first recovered clock, the second recovered clock, and the reference clock (for Channel 2, processing side, uses the second recovered clock and the channel word clock (the reference clock)) for subsequent processing of one of the first and second serial stream data (see Fig. 7 control of DMUX 708 that s/p converts the retimed serial data RXD2).

Desai does not expressly teach: delay locked loop circuitry.

In the same field of endeavor (processing serial data and CDR) Tang et. al., disclose: delay locked loop circuitry (see Fig. 7, 703 clock recovery DLL, part of dual loop retimer see paragraphs [0036]-[0041]).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Desai based on the teachings of Tang et. al., so that the clock recovery circuit of Desai comprises a delay-locked loop circuit, (such as the clock recovery system of Tang et. al.) that has minimum jitter generation and maximum jitter suppression (Tang et.al., [0013] and [0041]).

11. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mann et. al., (U.S. 5,251,210) in view of Tang et. al., (U.S. 2002/0075981).

With respect to claim 3, With respect to claim 3, Mann et. al., disclose: further comprising circuitry (see Fig. 7, blocks 260, and 250 of Channel 2) for receiving second serial data and produces a second recovered clock from the second serial data (see Fig. 7. output of block 250, "CLK Recovery & Data Decoder", column 14, lines 27-28) in the transceiver provides the second serial data to the circuit portion and wherein the circuit portion (Fig. 7 (the receiver side), see circuit portion including block 240, fifos 210, (and blocks to the right of the fifos, see column 13, lines 54-67, column 14,lines 1-15, and the reference clock is clock RxCLK out of block 240, used to recombine the serial streams, see column 15, lines 34-39) uses one of the first recovered clock, the second recovered clock, and the reference clock for subsequent processing of one of the first and second serial stream data

Mann et. al., do not expressly teach: delay locked loop circuitry.

In the same field of endeavor (processing serial data and CDR) Tang et. al., disclose: delay locked loop circuitry (see Fig. 7, 703 clock recovery DLL, part of dual loop retimer see paragraphs [0036]-[0041]).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Desai based on the teachings of Tang et. al., so that the clock recovery circuit of Desai comprises a delay-locked loop circuit, (such as the clock recovery system of Tang et. al.) that has minimum jitter generation and maximum jitter suppression (Tang et.al., [0013] and [0041]).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is 571 272 5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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